

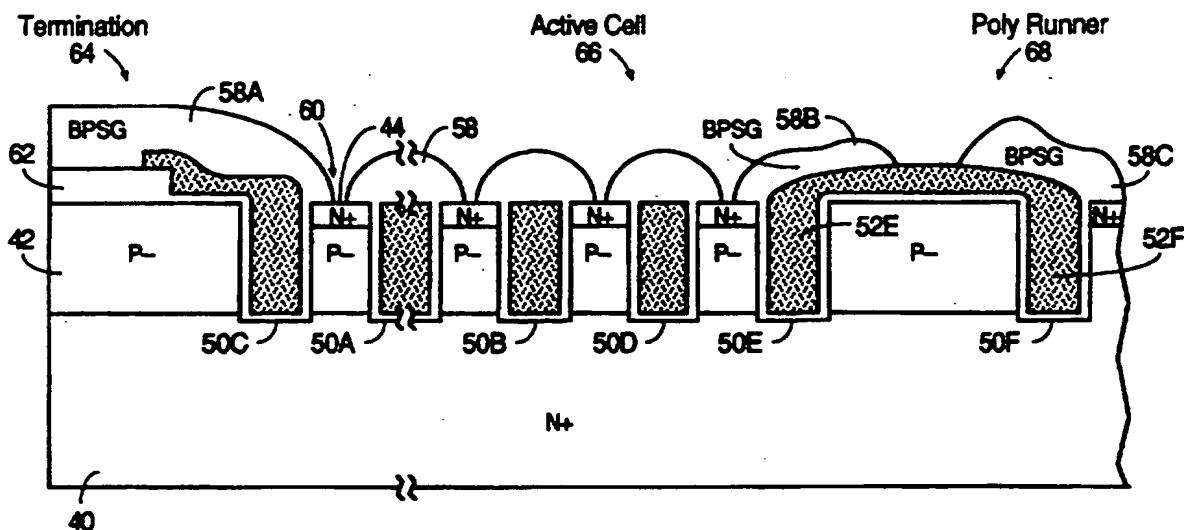


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(54) Title: PUNCH-THROUGH FIELD EFFECT TRANSISTOR



(57) Abstract

A trenched field effect transistor suitable especially for low voltage power applications provides low leakage blocking capability due to a gate controlled barrier region between the source region (44) and drain region (40). Forward conduction occurs through an inversion region between the source region (44) and drain region (40). Blocking is achieved by a gate controlled depletion barrier. Located between the source (44) and drain (40) regions is a fairly lightly doped body region (42). The gate electrode (52A), located in a trench (50A), extends through the source (44) and body (42) regions and in some cases into the upper portion of the drain region (40). The dopant type of the polysilicon gate electrode (52A) is the same type as that of the body region (42). The body region (42) is a relatively thin and lightly doped epitaxial layer grown upon a highly doped low resistivity substrate of opposite conductivity type. In the blocking state the epitaxial body region is depleted due to applied drain-source voltage, hence a punch-through type condition occurs vertically. Lateral gate control increases the effective barrier to the majority carrier flow and reduces leakage current to acceptably low levels.

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PUNCH-THROUGH FIELD EFFECT TRANSISTOR

BACKGROUND OF THE INVENTION5 FIELD OF THE INVENTION

This invention relates to semiconductor devices and more particular to a trenched field effect transistor especially suitable for low voltage switching applications.

10

DESCRIPTION OF THE PRIOR ART

Field effect transistors (FETs) are well known, as are metal oxide semiconductor field effect transistors (MOSFETs); such transistors are often used for power 15 applications. There is a need for power transistors for relatively low voltage applications, i.e. typically under 50 volts, that have low current leakage blocking capability.

Examples of trench field effect transistors suitable for such applications are disclosed in "Comparison of Ultra Low Specific On Resistance UMOSFET Structures..." by Syau et al., IEEE Transactions on Electron Devices, Vol. 41, No. 5, May 1994. Inter alia, this publication describes the so-called INVFET structure of present Figure 1, which corresponds to Figure 1(b) of the publication. Present Figure 1 shows only a portion of a single transistor including the polysilicon (polycrystalline silicon) gate electrode 10 which in this case is N-type polysilicon which is insulated by a gate oxide layer 12 on its sides and bottom in a trench 14 and insulated on its top side by an oxide layer 18. The trench 14 extends through the N+ doped source region 22 through the P doped base region 24 and into the N+ doped drain region 26. The drain electrode 30 is formed on the underside of the drain region 26 and the source electrode 32 formed on the top side of the source region.

Also described in Figure 1(c) of this article and shown here in present Figure 2 is the somewhat similar so-called EXTFET which is identical to the INVFET except for having an additional N- doped drift region 36 formed underlying the P doped base region 24. For both of these devices the P base region 24 is formed by diffusion (hence does not exhibit uniform doping) and is fairly heavily doped. It is believed that a typical surface concentration of the P base region 24 is 10¹⁷/cm³.

These devices are both intended to avoid full depletion of the P base (body) region 24. They each have the gate electrode 10 doped to the same conductivity type as is the drain region 26 (i.e. N type) as shown in Figures 1 and 2. The "mesa" width, i.e. the width of the source region between two adjacent trenches, is typically 3 μm and a typical cell pitch for an N-channel device is about 6 μm . Blocking is accomplished by a quasi-neutral (undepleted) PN junction at a V_{gs} (gate source voltage) of zero. The ACCUFET (see Syau et al. article) offers the best specific on resistance at the expense of poor blocking capability, while the INVFET and EXTFET offer improved blocking at the expense of increased specific on resistance.

As is well known, a power MOSFET should have the lowest possible on-state specific resistance in order to minimize conduction losses. On-state resistance is a well known parameter of the efficiency of a power transistor and is the ratio of drain-to-source voltage to drain current when the device is fully turned on. On-state specific resistance refers to resistance times cross sectional area of the substrate carrying the drain current.

However, these prior art devices do not provide the optimum low on-state specific resistance in combination with blocking state low current leakage.

5 SUMMARY

This disclosure is directed to a MOS semiconductor device suitable especially for low voltage power application where low leakage blocking capability is desirable. In accordance with the invention, the off-state blocking of a trenched field effect transistor is achieved by a gate controlled barrier region between the source and drain. Similar to the above described INVFET, forward conduction occurs through an inversion region between the source and the drain (substrate).
10 Unlike the INVFET, however, blocking is achieved by a gate controlled depletion barrier and not by a quasi-neutral PN junction. The depletion barrier is formed and controlled laterally and vertically so as to realize the benefits of ultra-low on-state specific
15 resistance combined with the low current leakage blocking. Advantageously, this structure is relatively easily fabricated and has blocking superior to that of prior art ACCUFET devices, with low leakage current at zero applied gate-source voltage. Moreover, in the
20 blocking state there is no quasi-neutral PN junction,
25 and therefore, like the ACCUFET, this structure offers the advantage of containing no parasitic bipolar PN junction.

The present device's on-state specific resistance
30 is comparable to that of the ACCUFET, and like the ACCUFET offers on-state specific resistance superior to that of the INVFET and EXTFET as described in the above mentioned article by Syau et al.

In an N-channel embodiment of the present
35 invention, an N+ drain region underlies a lightly doped P- body region which is overlain by an N+ source

region. The body region is formed by lightly doped epitaxy with uniform or almost uniform doping concentration, typically in a range of 10^{14} to $10^{16}/\text{cm}^3$. The gate electrodes are formed in trenches which extend through the source region, through the body region, and partially into the drain (substrate) region. Alternatively, the gate electrodes do not extend into the drain region. The polysilicon gate electrodes themselves are P doped, i.e. having a doping type the same as that of the body region. Additionally, the mesas (holding the source regions) located between adjacent gate electrode trenches are less than $1.5 \mu\text{m}$ wide, and the cell pitch is less than $3 \mu\text{m}$.

Advantageously in the blocking state the epitaxial P body region is depleted due to the applied drain-source bias V_{ds} , and hence a punch-through type condition occurs vertically. However, lateral gate control combined with the narrow mesa width (under $1.5 \mu\text{m}$) increases the effective depletion barrier to majority carrier flow and prevents conduction. Thus, the present device is referred to herein as the PT-FET for "punch-through field effect transistor".

Thus the blocking characteristics are determined by barrier-limited majority-carrier current flow and not by avalanche breakdown. In accordance with the invention, a complementary P-channel device is implemented and has advantages comparable to those of the above described N-channel device.

The above described embodiment has a floating body region, thus allowing bidirectional operation. In another embodiment a body contact region is provided extending into the body region from the principal surface of the semiconductor structure, thus allowing a source region to body region short via the source metallization for forward blocking-only applications.

Thus advantageously the present PT-FET has a fully depleted (punch-through) lightly doped body region at a small applied drain-source voltage. This differs from the P body region in the above described INVFET and 5 EXTFET which must, by design, be undepleted to avoid punch-through. Advantageously, the threshold voltage is low due to the lightly doped P body region and the device has an on-state specific resistance similar to that of the ACCUFET and superior to that of the INVFET 10 or EXTFET.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a prior art INVFET.

Figure 2 shows a prior art EXTFET.

15 Figure 3 shows an N-channel PT-FET in accordance with the present invention.

Figure 4A shows operation of the present PT-FET in equilibrium.

20 Figure 4B shows operation of the present PT-FET in the blocking (off) state with an applied drain-source voltage.

Figure 4C shows operation of the present PT-FET in the on state.

25 Figure 5 shows dimensions and further detail of one embodiment of a PT-FET.

Figures 6, 7 and 8 show three termination and poly runner structures suitable for use with the present PT-FET.

30 Figures 9A, 9B and 9C show process steps to fabricate a PT-FET in accordance with the present invention.

Figures 10A and 10B show two top side layouts for a PT-FET.

Figure 11 shows a P-channel PT-FET.

Figure 12 shows another embodiment of a PT-FET with a body contact region and the body region shorted to the source.

Similar reference numbers herein in various figures refer to identical or similar structures.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 3 shows a cross section (not to scale) of a portion of a trenched N-channel PT-FET in accordance with the present invention. It is to be understood that Figure 2, like the other figures herein, is not to scale and that furthermore the various doped semiconductor regions shown herein, which are illustrated as precisely defined regions delineated by borderlines, are conventional representations of doped regions having in reality gradient dopant levels at their edges. Moreover, as is well known in the art and as described further below, typically power MOSFETs include a large number of cells, the cells having various shapes such as square, circular, hexagonal, linear or others. These cells are evident in a top side view, several of which are provided below. In terms of cell layout, the PT-FET is conventional and may be fabricated in any one of a number of well known cell structures. The present illustrations are therefore typically of only one cell or a portion of two cells as delineated by the gate trenches, and are not intended to illustrate an entire power transistor which would typically include hundreds or thousands of such cells.

Moreover, certain well known elements of such trenched MOSFETs are not shown in certain of the present drawings. For instance, the metallization which connects to the gate electrodes is typically not shown as being outside the plane of the present cross sectional drawings. Also, the termination portions of

the transistors are only shown in certain of the drawings below; in others the termination portions are outside the area depicted in the drawings.

Figure 3 shows one embodiment of an N-channel PT-FET including a drain (substrate) region 40 which is N+ doped to have a resistivity of e.g. 0.002 Ω-cm. Formed immediately over the drain region 40 is a P- doped body region 42 having a doping concentration in the range of e.g. 10^{14} to $10^{16}/\text{cm}^3$ and a typical doping concentration of $10^{15}/\text{cm}^3$.

Overlying the body region 42 is the N+ doped source region 44 which is doped to a concentration of e.g. $2 \times 10^{19}/\text{cm}^3$. A conventional metallized drain contact 48 is formed the backside of the semiconductor substrate. Formed in the upper portion of the semiconductor structure are trenches 50A, 50B, which respectively hold P+ doped polysilicon gate electrodes 52A, 52B which are each doped P-type to a maximum attainable value. (It is to be understood that gate electrodes 52A, 52B are connected to each other outside the plane of the drawing). Each trench 50A, 50B is lined with gate oxide layer 54 e.g. 500 Å thick (a typical range is 400 to 800 Å) to insulate the polysilicon gate electrodes from the silicon sidewalls and bottom of the trenches 50A, 50B.

Not depicted in this illustration are the passivation layer (typically boro-phosphosilicate glass BPSG) and the top side source contact metallization. In this case the body region 42 is a "floating region", having no electrical contact made thereto. This structure has been found especially suitable for high current, low voltage switching applications, i.e. less than 25 volts.

The principle of operation of this device is illustrated in Figures 4A, 4B and 4C. Figure 4A illustrates equilibrium, and Figure 4B illustrates

operation in the blocking (off) state. Thus the gate-source bias voltage (V_{gs}) is equal to zero in both Figures 4A and 4B. In the blocking state the drain-source voltage (V_{ds}) is greater than or equal to zero, 5 since operation of the device of Figure 3 is bidirectional. Figure 4A illustrates the body depletion for the situation where the drain-source voltage is equal to zero. (It is to be understood that there is plus (+) charge depletion in the N+ source and 10 drain regions which is not drawn for simplicity.) This is an equilibrium state in terms of the charge distribution, as shown in Figure 4A.

In Figure 4B, the drain-source voltage is greater than zero while the gate-source voltage is still equal 15 to zero. In this case the body region is fully depleted. The leakage current is controlled by an electron energy barrier formed within the body depletion region as shown. The leakage current is reduced to acceptably low levels (e.g., 1% of that of 20 an ACCUFET) by the P-doped polysilicon gate electrodes 52A, 52B. It has been found by the present inventors that a P-type polysilicon gate electrode for an N-channel device (that is, the polysilicon gate electrode having the same conductivity type as the adjacent body 25 region) is highly beneficial. The P-type polysilicon gate electrode allows the body region to remain fully depleted while it enhances the energy barrier to reduce leakage to acceptable levels (levels superior to those of the ACCUFET).

30 Thus majority carrier current flow is provided without any deleterious PN junction behavior. There is also no need to short the source region 44 to the body region 42, hence allowing bidirectional operation of the PT-FET. Thus the gate control of the barrier 35 allows low current leakage, superior to that of the

prior art ACCUFET, because the barrier is larger due to the doping type of the lightly doped body region 42.

Figure 4C illustrates the on state conduction which is typically the situation with the gate-source voltage being greater than the transistor threshold voltage and the drain-source voltage is greater than zero.

In this case as shown the inversion regions are along the trench 50A, 50B side walls which conduct majority carrier through the inversion region. Current flow takes place when the drain-source voltage is greater than zero, in the direction shown by the arrow. Advantageously the lightly doped body region 42 allows a low threshold voltage, while in addition the on-state specific resistance is superior to that of the INVFET or the EXTFET, and comparable to that of the ACCUFET.

Figure 5 shows additional detail of an N channel PT-FET which is otherwise similar to that of Figures 3 and 4. Also illustrated in Figure 5 is the conventional (passivation) layer 58 which is BPSG overlying each polysilicon gate electrode, and the metal, e.g. aluminum, source contact. Also shown in Figure 5 are exemplary dimensions for the gate oxide 54 thickness (500 Å) and the source region 44 thickness (0.25 μm). The typical trench 50A, 50B depth is 2.1 μm, which extends through the source region 44 and body region 42 and partially into the substrate region 40. An exemplary thickness of the substrate (drain region 40) is 500 μm.

As illustrated, the mesa (the silicon between two adjacent gate trenches) is e.g. 1 μm (under 1.5 μm) in width while each trench 50A, 50B is 1 μm (under 1.5 μm) in width, thus allowing an exemplary 2 μm to 3 μm pitch per cell.

Figures 3, 4 and 5 each only illustrate one cell or a portion of two cells in the active portion of a

typical multi-cell PT-FET. Figure 6 illustrates a first embodiment of a PT-FET with at the left side a termination region 64. At the right side is a "poly runner" region 68 for contacting low-resistivity metal 5 (not shown) to the relatively higher resistivity gate electrode material. Figure 6 shows a number of cells (additional cells are omitted, as suggested by the broken lines) in the active region of the device. The left side termination region 64 includes, adjacent the 10 leftmost trench 50C, the absence of any N+ source region. Also present in termination region 64 is a BPSG layer 58A. Source contact 60 is located between BPSG portions 58A, 58. In the right side poly runner region 68 (mesa), again there is no source region to 15 the right of trench 50E. This mesa provides a wide contact region for running metallization to select regions of polysilicon for the purpose of lowering total gate resistance. Also shown in Figure 6 is field oxide region 62 in termination region 64, underlying 20 BPSG layer 58A. Optionally the field oxide is also present in the poly runner region 68. Polysilicon structure 52F includes a gate runner to the polysilicon gate electrode 52E of the adjacent cell in trench 50E.

Figure 7 shows a second PT-FET having a 25 termination region and poly runner region which differ from those of Figure 6 in two ways. First, P+ regions 62A, 62B are provided in both the left side termination and right side poly runner regions 64, 68. These P+ regions 62A, 62B prevent leakage in the relatively wide 30 poly runner region 68 and prevent inversion in both the termination 64 and poly runner regions 68.

Additionally, the N+ source regions 44A, 44B are 35 present respectively in the termination and poly runner regions. In this case the polysilicon ("poly") runner in the right side poly runner region 68 extends over to contact the N+ region 44B in the poly runner region 68,

with a contact 60B made to that N+ region for purposes of electrostatic (ESD) robustness.

Figure 8 shows a third PT-FET similar to that of Figure 7 in having the N+ regions 44A, 44B respectively 5 in the termination and poly runner regions, but not having a P+ region in the termination or poly runner regions. Additionally the N+ region 44B in the right side poly runner region 68 does not have an exterior metallized contact (is floating) to prevent leakage in 10 the relatively wide mesa region. Figure 8 is similar to Figures 6 and 7 in that polysilicon structure 52F includes a runner to the gate electrode 52E in adjacent trench 50E.

A process for fabricating an N-channel PT-FET is 15 illustrated in Figures 9A through 9C. Beginning in Figure 9A, an N+ doped silicon substrate 40 (having a resistivity e.g. 0.001 - 0.005 Ω-cm) is provided, on which is grown epitaxially a lightly doped P- region 42 having a doping concentration of $10^{15}/\text{cm}^3$ which becomes 20 the body region. A typical final thickness of this P-epitaxial layer 42 after all processing is 2 μm.

Then in several steps shown in Figure 9B, an active region mask (not shown) is formed over the principal surface of the epitaxial layer 42 to pattern 25 the field oxide in the termination region and optionally in the poly runner region. The active region mask patterns the field oxide in the termination region and opens the areas for active cells. Next a source mask is formed and patterned, and then through 30 the openings in the source mask the N+ source region 44 is implanted and diffused to a thickness (depth) of approximate 0.25 μm and a final surface doping concentration of e.g. $2 \times 10^{19}/\text{cm}^3$. The N+ source region 44, due to the source region mask, is not implanted in 35 the termination 64 and poly runner regions 68 (as shown in Figure 6 for instance) in some embodiments. In the

embodiments of Figures 7 and 8 the N⁺ source region implant is a maskless step which occurs before the field oxide/active mask steps. In the embodiment of Figure 6, the source region implant occurs after the 5 active mask steps.

Then in several steps in Figure 9C, the upper surface of the P-doped epitaxial layer 42 is masked and the mask is patterned to define the trench locations. The trenches are then conventionally anisotropically 10 etched by e.g. dry etching to a depth of approximately 2.1 μm.

After the trenches are etched, a gate oxide layer 54 e.g. 500 Å thick (in a range of 400 to 800Å) is formed lining the trenches and over the entire surface 15 of the epitaxial layer 42.

Then a layer of polysilicon is deposited filling the trenches and over the entire surface of the epitaxial layer. The polysilicon is then heavily doped with a P type dopant before it is patterned. A mask is 20 then applied to the upper surface of the polysilicon and the mask is patterned and the polysilicon etched to define the gate electrodes and the polysilicon runners (as described above) connecting the gate electrodes.

In the embodiment of Fig. 7, the P⁺ region 62A, 25 62B is implanted using a mask by e.g. a high energy implant, either before or after the trenches are etched and filled.

After patterning of the polysilicon gate structures 52A, 52B, a layer of BPSG 58 is formed 30 thereover and subsequently patterned using a mask to define the contact openings to the silicon surface.

Then the metallization layer is deposited and conventionally patterned using a mask. Then 35 conventionally a final e.g. PSG or nitride passivation layer (not shown) is formed and masked to define the contact pads.

Figure 10A illustrates a top side view of a portion of the PT-FET in accordance with one embodiment. In this case the cells are rectangular and isolated by the trenches, the small rectangles being the source regions 70-1 . . . , 70-n. Hence the trenches are formed in a criss-cross pattern to define the rectangular cells. The mesa region 82 surrounding the cells is the termination region as in Figs. 6-8.

Figure 10B shows alternatively a linear cell type arrangement where the trenches, while criss-crossing, have a different spacing in the left-right direction than they do in the vertical direction in the drawing. This represents a linear open-cell geometry with source regions 72-1, 72-2, . . . , 72-n each isolated by the trenches and termination mesa region 82.

Figure 11 depicts the P-channel complement of the PT-FET of Figure 3. This PT-FET has all conductivity types opposite to that of the PT-FET of Figure 3. Shown are drain region 82, body region 84, source region 86, and N+ doped gate electrodes 88A, 88B. Similarly, in the termination region (not shown) the conductivity types are complementary to those of Figure 3. The dimensions of the PT-FET of Figure 11 would be similar to those of Figure 5, as is the doping concentration for each particular region within well known material constraints.

Figure 12 shows another embodiment of an N-channel PT-FET which in most respects is identical to that of Figure 3, but has the addition of a P+ doped body contact region 92 formed in an upper portion of the semiconductor structure. This allows, via a conventional source-body contact (not shown in Figure 12), the shorting of the source region 44 to the body region 42. This prevents bidirectional operation and so provides a device which operates with forward conductivity only.

The above description is illustrative and not limiting; further modifications will be apparent to one skilled in the art in light of this disclosure and are intended to fall within the scope of the appended 5 claims.

IN THE CLAIMS

1. A semiconductor device, comprising:
 - a drain region of a first conductivity type and uniform doping concentration;
 - 5 a body region of a second opposite conductivity type formed overlying and in direct contact with the drain region;
 - a source region of the first conductivity type formed overlying the body region; and
 - 10 a conductive gate electrode extending into at least the source region and the body region, wherein the gate electrode is polycrystalline silicon doped to the second conductivity type;
 - 15 wherein the device has three external independent electrodes to respectively the source region, the gate electrode, and the drain region.
2. The semiconductor device of Claim 1, wherein the body region is of uniform doping concentration.
3. The semiconductor device of Claim 1, wherein a doping concentration of the body region is less than $10^{16}/\text{cm}^3$.
- 25 4. The semiconductor device of Claim 3, wherein a doping concentration of the body region is about $10^{15}/\text{cm}^3$.
- 30 5. The semiconductor device of Claim 1, wherein the body region is electrically floating, thereby not in electrical contact with any structures except the source region and drain region.
- 35 6. The semiconductor device of Claim 1, further comprising a body contact region of the second

conductivity type formed in the body region and laterally adjacent the source region.

7. The semiconductor device of Claim 6, further
5 comprising a body electrode in contact with the body contact region.

8. The semiconductor device of Claim 1, further comprising a drain electrode in contact with the drain
10 region.

9. The semiconductor device of Claim 1, further comprising a second gate electrode laterally spaced apart from the gate electrode by less than about 1.5
15 μm .

10. The semiconductor device of Claim 1, wherein
a total thickness of the source region and body region
is about 2 μm .
20

11. The semiconductor device of Claim 9, wherein
the gate electrode has a lateral width of about 1 μm .

12. The semiconductor device of Claim 1, further
25 comprising a termination region laterally surrounding
an active region of the device, the termination region including a conductive structure extending in a trench into the body region and over a principal surface of the body region.
30

13. The semiconductor device of Claim 12, further comprising a runner area adjacent an active portion of the device, the runner region including a conductive structure extending in a trench into the body region
35 and over a principal surface of the body region, and being in contact with the conductive gate electrode.

14. The semiconductor device of Claim 13, wherein
the termination region and runner regions each further
includes a doped region of the second conductivity type
and being more heavily doped than the body region and
5 overlying the body region in respectively the
termination region and the runner region.

15. The semiconductor device of Claim 14, wherein
a doping level of the doped region in the termination
10 region and in the runner region is in a range of 10^{17} to
 $10^{19}/\text{cm}^3$.

16. The semiconductor device of Claim 1, wherein
the conductive gate electrode extends into the drain
15 region.

17. A semiconductor device comprising;
a drain region of a first conductivity type
and uniform doping concentration;
20 a body region of a second conductivity type
and being of uniform doping concentration
overlying and being in direct contact with the
drain region, and having a doping concentration of
less than $10^{16}/\text{cm}^3$;
25 a source region of the first conductivity
type overlying the body region; and
a gate electrode of polycrystalline silicon
doped to have the second conductivity type and
extending through the source region into the body
30 region; wherein the device has three external
independent electrodes to respectively the source
region, the gate electrode, and the drain region.

18. The semiconductor device of Claim 17, further
35 comprising a second gate electrode extending into the
body region and laterally spaced apart from the first

gate electrode less than about 1.5 μm in the body region.

19. The semiconductor device of Claim 1, wherein
5 when the semiconductor device is in a blocking state,
whereby the gate electrode to source region voltage is
equal to zero, the body region is electrically
depleted.

10 20. A semiconductor device, comprising:
 an active portion including:
 a drain region of a first conductivity
 type;
 a body region of a second opposite
15 conductivity type formed overlying and in
 contact with the drain region;
 a source region of the first
 conductivity type formed overlying the body
 region;
20 a conductive gate electrode extending
 into at least the source region and the body
 region, wherein the gate electrode is
 polycrystalline silicon doped to the second
 conductivity type;
25 a termination region laterally
 surrounding the active region of the device,
 the termination region including a conductive
 structure extending in a trench into the body
 region and over a principal surface of the
 body region; and
30 a runner region adjacent the active
 portion of the device, the runner region
 including a conductive structure extending in
 a trench into the body region and over a
 principal surface of the body region, and
35

being in contact with the conductive gate electrode;

wherein the termination region and runner regions each includes a doped region of the second conductivity type and being more heavily doped than the body region, and overlying the body region in respectively the termination region and the runner region.

AMENDED CLAIMS

[received by the International Bureau on 6 August 1996 (06.08.96);
new claims 21-38 added; remaining claims unchanged (7 pages)]

1. A semiconductor device, comprising:
 - 5 a drain region of a first conductivity type and uniform doping concentration;
 - 10 a body region of a second opposite conductivity type formed overlying and in direct contact with the drain region;
 - 15 a source region of the first conductivity type formed overlying the body region; and a conductive gate electrode extending into at least the source region and the body region, wherein the gate electrode is polycrystalline silicon doped to the second conductivity type; wherein the device has three external independent electrodes to respectively the source region, the gate electrode, and the drain region.
2. The semiconductor device of Claim 1, wherein the 20 body region is of uniform doping concentration.
3. The semiconductor device of Claim 1, wherein a doping concentration of the body region is less than $10^{16}/\text{cm}^3$.
25
4. The semiconductor device of Claim 3, wherein a doping concentration of the body region is about $10^{15}/\text{cm}^3$.
5. The semiconductor device of Claim 1, wherein the 30 body region is electrically floating, thereby not in electrical contact with any structures except the source region and drain region.
6. The semiconductor device of Claim 1, further comprising a body contact region of the second conductivity type formed in the body region and laterally adjacent the
35

source region.

7. The semiconductor device of Claim 6, further comprising a body electrode in contact with the body contact region.

8. The semiconductor device of Claim 1, further comprising a drain electrode in contact with the drain region.

9. The semiconductor device of Claim 1, further comprising a second gate electrode laterally spaced apart from the gate electrode by less than about 1.5 μm .

10. The semiconductor device of Claim 1, wherein a total thickness of the source region and body region is about 2 μm .

11. The semiconductor device of Claim 9, wherein the gate electrode has a lateral width of about 1 μm .

12. The semiconductor device of Claim 1, further comprising a termination region laterally surrounding an active region of the device, the termination region including a conductive structure extending in a trench into the body region and over a principal surface of the body region.

13. The semiconductor device of Claim 12, further comprising a runner area adjacent an active portion of the device, the runner region including a conductive structure extending in a trench into the body region and over a principal surface of the body region, and being in contact with the conductive gate electrode.

14. The semiconductor device of Claim 13, wherein the

termination region and runner regions each further includes a doped region of the second conductivity type and being more heavily doped than the body region and overlying the body region in respectively the termination region and the 5 runner region.

15. The semiconductor device of Claim 14, wherein a doping level of the doped region in the termination region and in the runner region is in a range of 10^{17} to $10^{19}/\text{cm}^3$.

10

16. The semiconductor device of Claim 1, wherein the conductive gate electrode extends into the drain region.

15

17. A semiconductor device comprising;
a drain region of a first conductivity type and uniform doping concentration;

20

a body region of a second conductivity type and being of uniform doping concentration overlying and being in direct contact with the drain region, and having a doping concentration of less than $10^{16}/\text{cm}^3$;

a source region of the first conductivity type overlying the body region; and

25

a gate electrode of polycrystalline silicon doped to have the second conductivity type and extending through the source region into the body region; wherein the device has three external independent electrodes to respectively the source region, the gate electrode, and the drain region.

30

18. The semiconductor device of Claim 17, further comprising a second gate electrode extending into the body region and laterally spaced apart from the first gate electrode less than about $1.5 \mu\text{m}$ in the body region.

35

19. The semiconductor device of Claim 1, wherein when the semiconductor device is in a blocking state, whereby the

gate electrode to source region voltage is equal to zero, the body region is electrically depleted.

20. A semiconductor device, comprising:
5 an active portion including:
 a drain region of a first conductivity type;
 a body region of a second opposite
 conductivity type formed overlying and in contact
 with the drain region;
10 a source region of the first conductivity
 type formed overlying the body region;
 a conductive gate electrode extending into
 at least the source region and the body region,
 wherein the gate electrode is polycrystalline
15 silicon doped to the second conductivity type;
 a termination region laterally surrounding
 the active region of the device, the termination
 region including a conductive structure extending
 in a trench into the body region and over a
 principal surface of the body region; and
20 a runner region adjacent the active portion
 of the device, the runner region including a
 conductive structure extending in a trench into
 the body region and over a principal surface of
 the body region, and being in contact with the
 conductive gate electrode;
 wherein the termination region and runner
25 regions each includes a doped region of the second
 conductivity type and being more heavily doped
 than the body region, and overlying the body
 region in respectively the termination region and
 the runner region.
- 30 21. A method of forming a semiconductor device,
 comprising the steps of:
 providing a semiconductor substrate heavily doped

to have a first conductivity type;

epitaxially forming a body layer doped to have a second opposite conductivity type directly on the substrate;

5 forming a source region heavily doped to have the first conductivity type in an upper portion of the epitaxial body layer;

forming a trench extending through the source region into the body layer;

10 forming a polycrystalline silicon structure in the trench; and

doping the polycrystalline silicon structure to the second conductivity type.

15 22. The method of Claim 21, wherein a doping concentration of the body layer is less than $10^{16}/\text{cm}^3$.

23. The method of Claim 21, further comprising the steps of:

20 forming a second trench extending through the source region into the body layer;

forming a second polycrystalline silicon structure in the trench; and

25 doping the second polycrystalline crystal structure to the second conductivity type;

wherein the second trench is laterally spaced apart from the first trench by less than 1.5 μm .

30 24. The method of Claim 21, wherein the body layer formed epitaxially is of uniform doping concentration.

25. The method of Claim 21, wherein a doping concentration of the body layer is in a range of 10^{14} to $10^{16}/\text{cm}^3$.

35

26. The method of Claim 21, wherein the source region

overlies all of the body layer and thereby the body layer is electrically floating, and thereby not in electrical contact with any structures except the source region and semiconductor substrate.

5

27. The method of Claim 21, further comprising the step of forming a body contact region of the second conductivity type in the body layer and laterally adjacent the source region.

10

28. The method of Claim 26, further comprising the step of forming a body electrode in contact with the body contact region.

15

29. The method of Claim 21, further comprising the step of forming a drain electrode in direct contact with the semiconductor substrate.

20

30. The method of Claim 21, further comprising the step of forming a second doped polycrystalline silicon structure in the substrate and laterally spaced apart from the doped polycrystalline silicon structure by less than 1.5 μm .

25

31. The method of Claim 21, wherein a total thickness of the source region and body layer is 2 μm .

30

32. The method of Claim 21, wherein the doped polycrystalline silicon structure has a lateral width of less than 1.5 μm .

35

33. The method of Claim 38, wherein the termination region and runner region each further includes a doped region of the second conductivity type and being more heavily doped than the body layer and overlying the body layer in respectively the termination region and the runner

region.

34. The method of Claim 34, wherein a doping level of the doped region in the termination region and in the runner 5 region is in a range of 10^{17} to $10^{19}/\text{cm}^3$.

35. The method of Claim 21, wherein the doped polycrystalline silicon structure in the trench extends into the substrate.

10

36. The method of Claim 21, further comprising the steps of:

15

forming a trench extending into the body layer and spaced apart from the source region, thereby being in a termination region of the semiconductor device; and

forming a conductive structure in the trench and laterally surrounding the source region and extending over a principal surface of the body layer.

20

37. The method of Claim 37, further comprising the steps of:

forming an additional trench into the body layer and spaced apart from the source region, thereby being in a runner region of the semiconductor device; and

25

forming a conductive structure in the additional trench and over a principal surface of the body layer, and being in contact with the doped polycrystalline silicon structure.

30

38. The method of Claim 21, there being no intervening region between the heavily doped substrate and the body layer.

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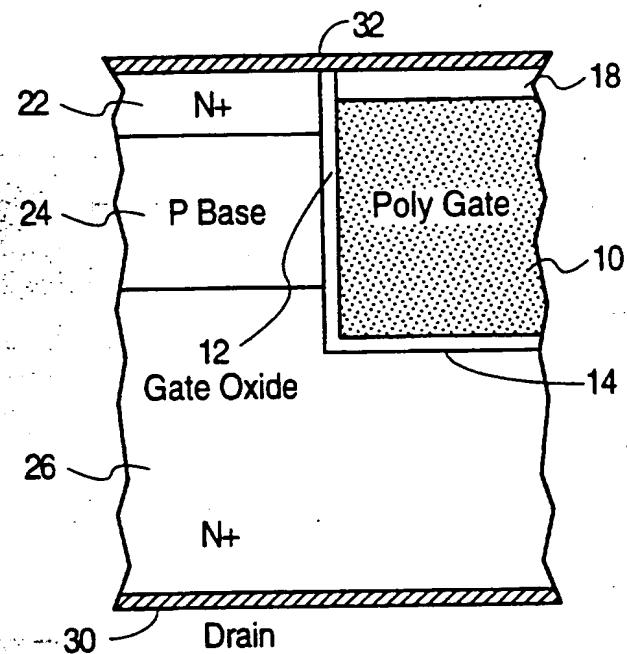


FIG. 1
(PRIOR ART)

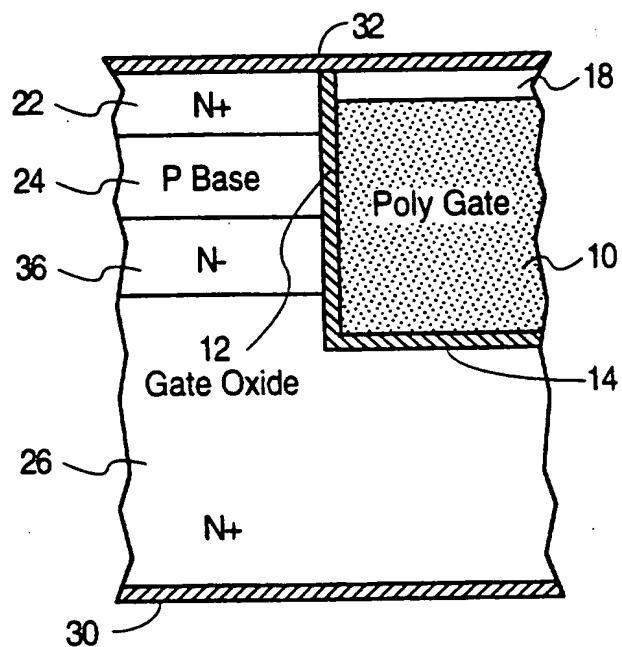


FIG. 2
(PRIOR ART)

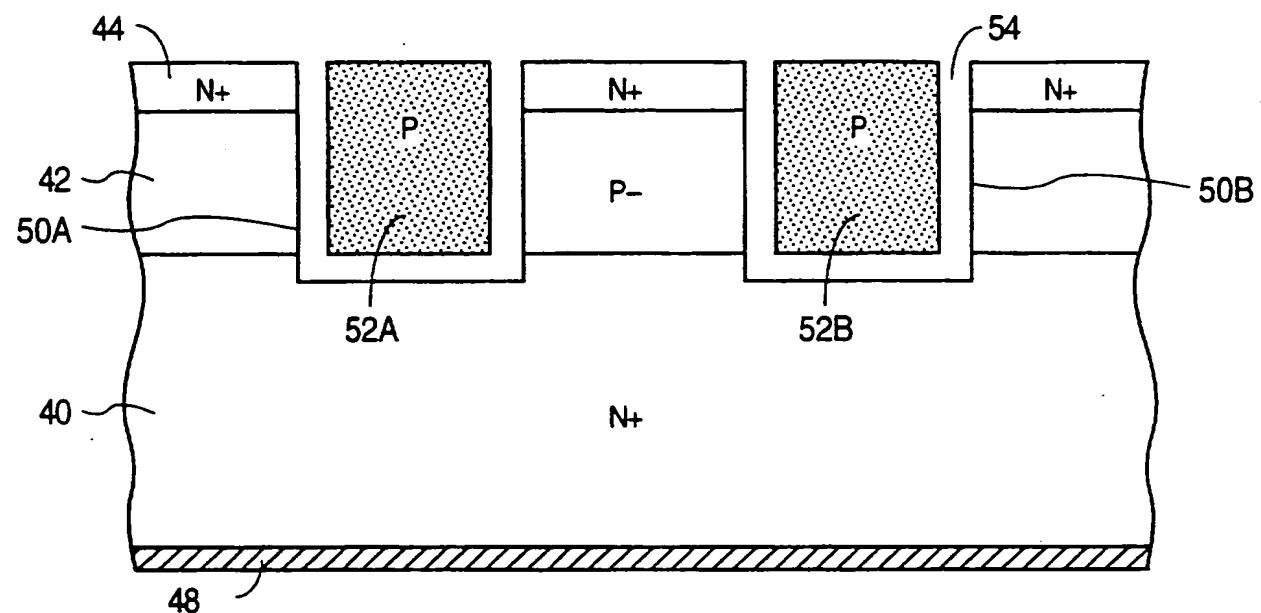


FIG. 3

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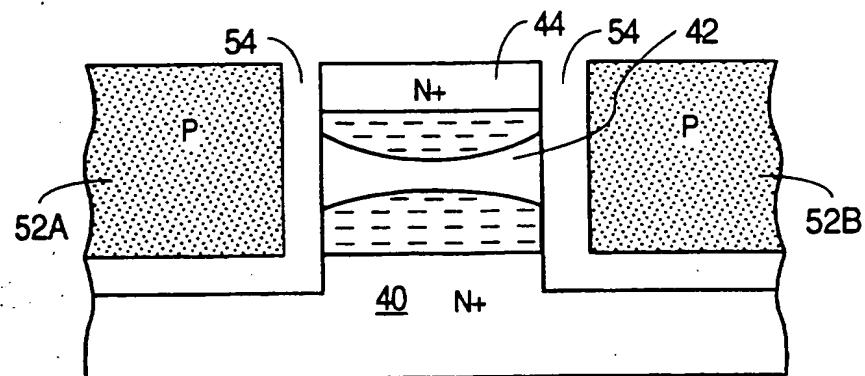


FIG. 4A

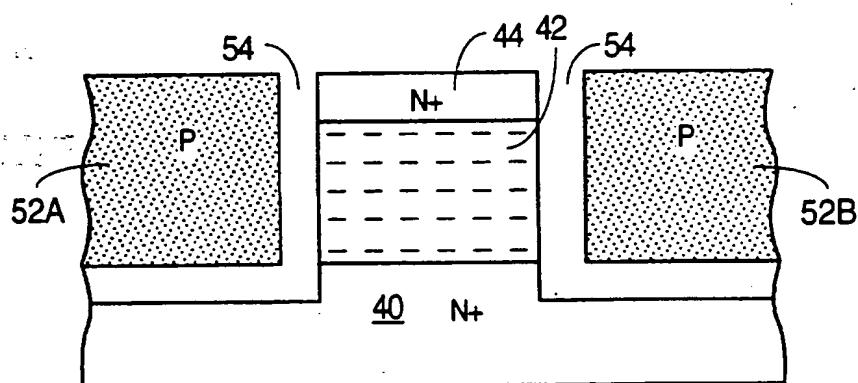


FIG. 4B

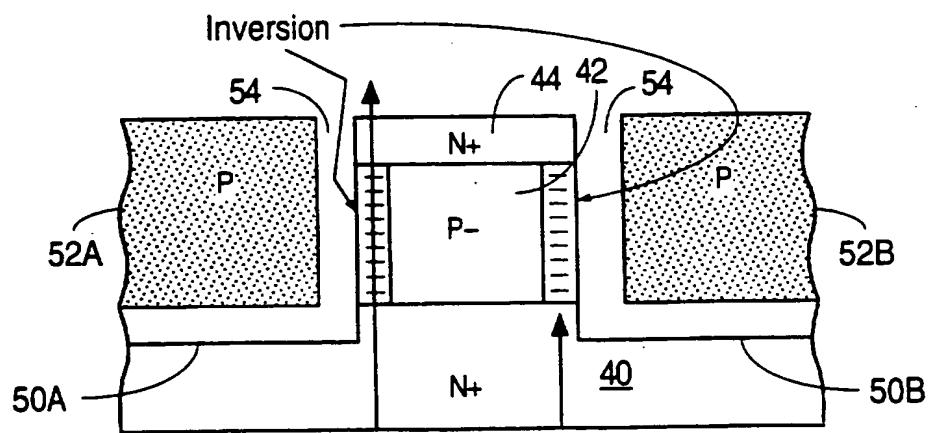


FIG. 4C

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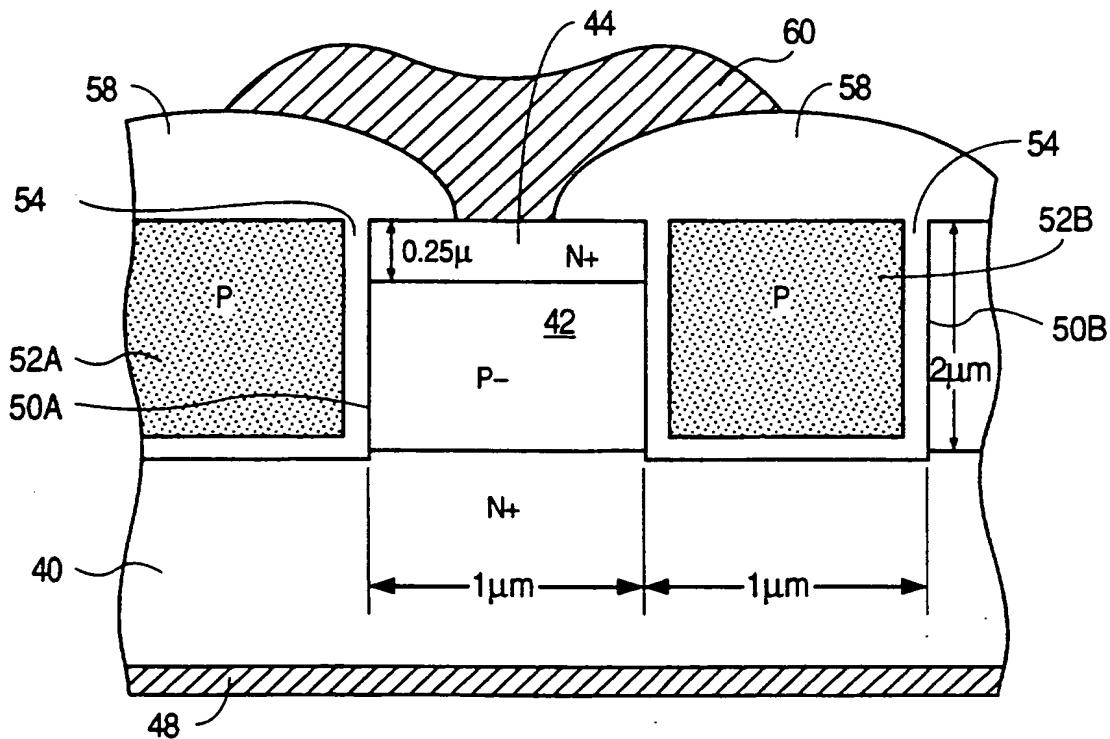
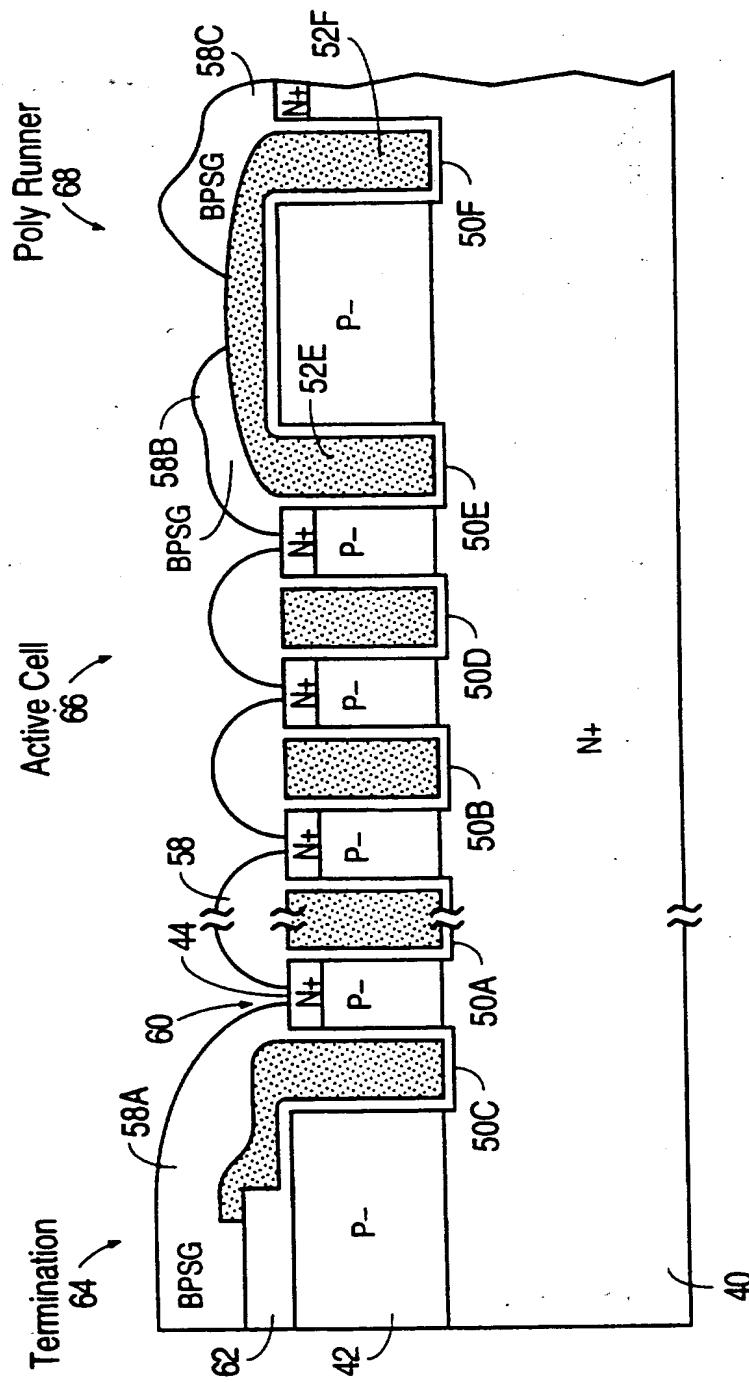


FIG. 5

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6
FIG.

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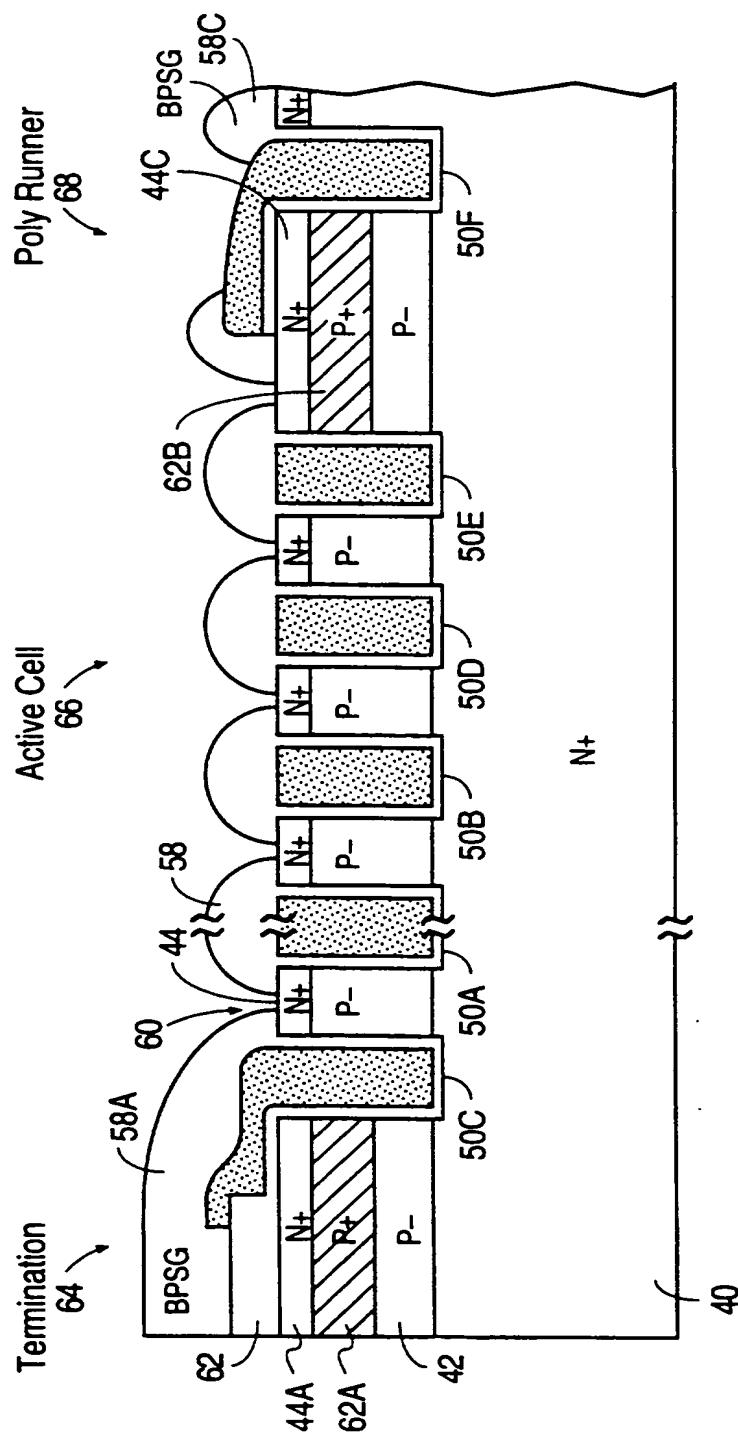


FIG. 7

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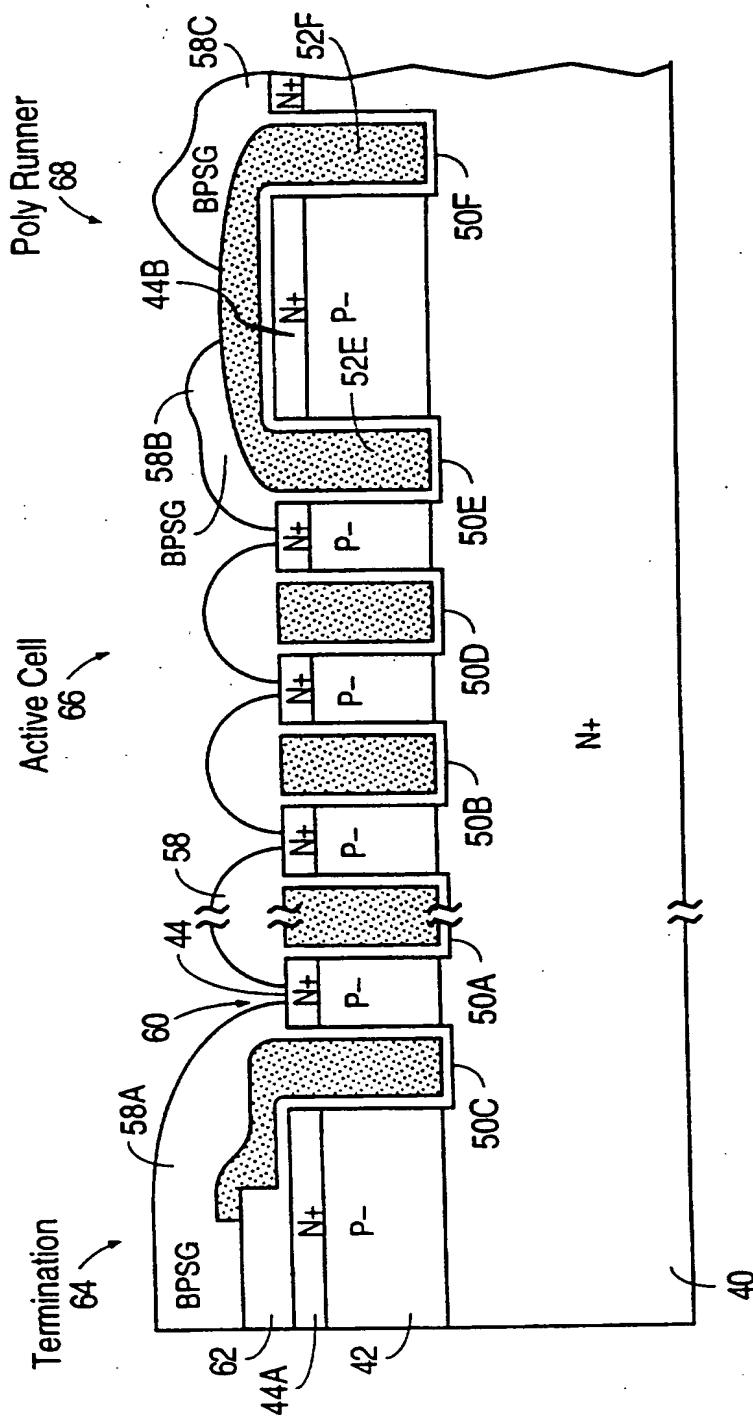


FIG. 8

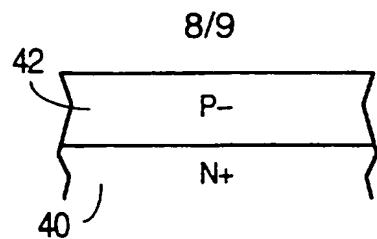


FIG. 9A

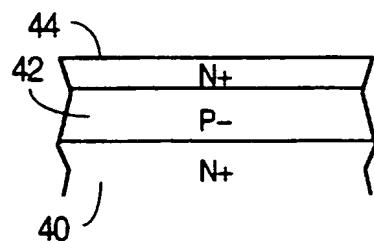


FIG. 9B

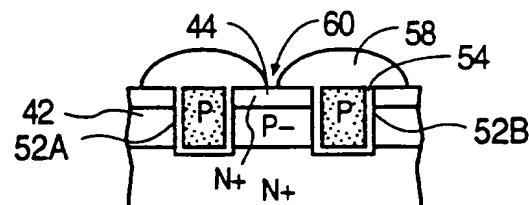


FIG. 9C

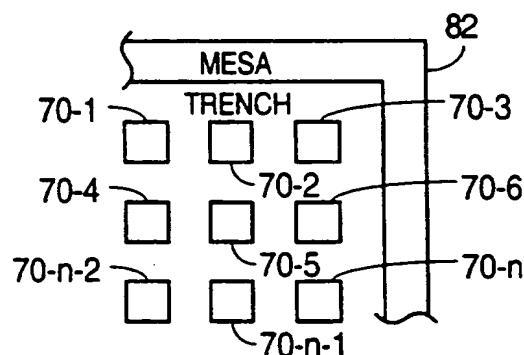


FIG. 10A

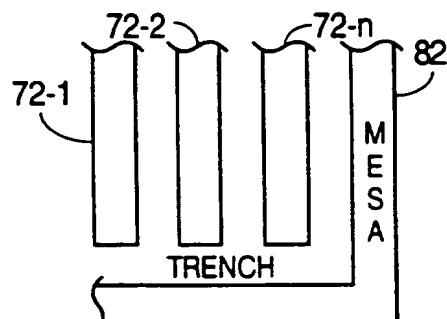


FIG. 10B

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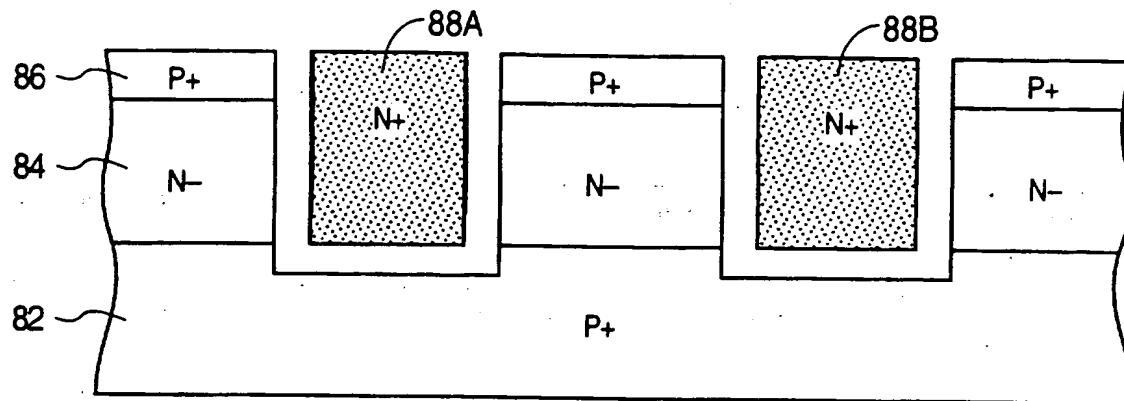


FIG. 11

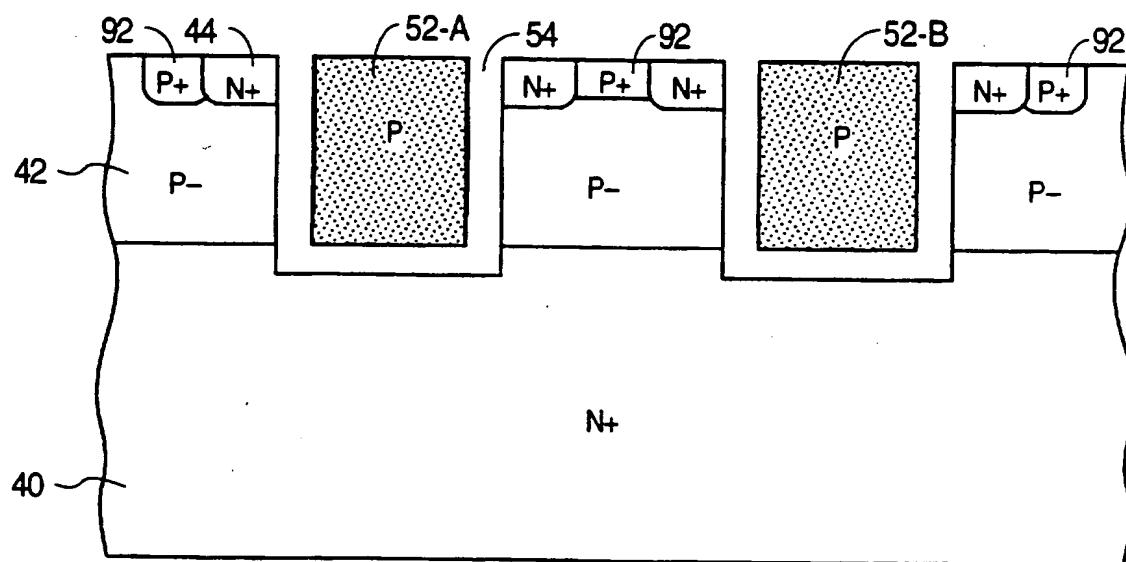


FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/03639

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) : HO1L 29/78, 745
US CL : 257/264,268,331,341,407,630

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/264,268,331,341,407,630

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A, 5,378,911 (Murakami) 03 January 1995, figures 17 and 18, col. 16 and 17.	1-11,16-19
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Y		12-15,20
Y	US,A, 5,316,959 (Kwan et al) 31 May 1994, See entire patent.	12-15,20
Y,P	US,A, 5,468,982 (Hshieh et al) 21 November 1995, figures 11-13, cols.6 and 7.	12-15,20
Y	US,A, 5,298,442 (Bulucea et al) 29 May 1994, figures 21-31, cols.11-16	12-15,20
A	US,A, 4,633,292 (Fellinger et al) 30 December 1986	

Further documents are listed in the continuation of Box C. See patent family annex.

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L document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
O document referring to an oral disclosure, use, exhibition or other means		
P document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search

29 MAY 1996

Date of mailing of the international search report

10 JUN 1996

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